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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,145	02/28/2002	Andrew Mark Nightingale	550-310	5033

7590 12/18/2003

NIXON & VANDERHYE P.C.  
8th Floor  
1100 North Glebe Rd.  
Arlington, VA 22201-4714

EXAMINER

LE, TOAN M

ART UNIT PAPER NUMBER

2863

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/084,145

Applicant(s)

NIGHTINGALE, ANDREW MARK

Examiner

Toan M Le

Art Unit

2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 February 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

Please label the blocks in figure 5.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-18 are rejected under 35 U.S.C. 102(a) as being anticipated by “Hardware Development of  $\mu$ PLAT”, Kishi et al. (referred hereafter Kishi et al.).

Referring to claim 1, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, the method comprising the steps of: (a) reading a configuration file containing predetermined parameters identifying the type of the device and capabilities of the device (figure 4, “config. file”); (b) employing a configuration engine to dynamically generate a test environment for the device by creating selected test components which are coupled via the bus with a representation of tile device to form the test environment, the test components being selected dependent on the configuration file (figure 4, “ $\mu$ PLAT core Test Bench”); (c) causing a test sequence to be executed (figure 4, “Test environment of  $\mu$ PLATcore-7C based system LSI”); and (d) monitoring signals passed between the representation of the device and one or more of the test components during execution of the test sequence to generate result data indicating compliance with the bus protocol (page 25, 1<sup>st</sup> column: Section 3.3 IP Product Line Up, lines 1-7; 2<sup>nd</sup> column, lines 1-2; page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

As to claim 2, Kishi et al. disclose a method of testing compliance of a device with a bus protocol (Table 2, "IEEE1394 Protocol"), wherein the configuration file is selected from a set of configuration file templates, the set containing a configuration file template for each type of device (figure 4, "Prog./Param. files"), and each configuration file having a number of entries for providing configuration information specific to the device (figure 4, "log file").

Referring to claim 3, Kishi et al. disclose a method of testing compliance of a device with a bus protocol (Table 2, "IEEE1394 Protocol"), wherein said step (d) comprises the step of employing a protocol checking component to check that signals passed between the representation of the device and one or more of the test components during execution of the test sequence do not violate a set of predetermined rules of the bus protocol (Table 2, "IEEE1394 Protocol").

As to claim 4, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein said step (d) comprises the step of employing a coverage monitoring component to monitor signals passed between the representation of the device and one or more of the test components during execution of the test sequence to determine whether a set of coverage points are observed (page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

Referring to claim 5, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the set of coverage points is configured dependent on the configuration file read at the step (a) (figure 4, "config. file").

As to claim 6, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the step (d) comprises the step of employing a protocol checking component to check that signals passed between the representation of the device and one or more of the test components during execution of the test sequence do not violate a set of predetermined rules of

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the bus protocol, and wherein, if all coverage points in the set have been observed without violating any of the set of predetermined rules of the bus protocol, the method further comprises the step of generating an output confirming compliance with the bus protocol (Table 2; page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

Referring to claim 7, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein at the step (b) the step of creating selected test components comprises selecting the test components to be created in dependence on the type of device to be tested (figure 4).

As to claim 8, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein at least one of the test components has associated therewith a plurality of behaviors that it may exhibit, the choice of behavior being determined when that test component is created dependent on the type of device to be tested (page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

Referring to claim 9, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the test sequence is a user-definable test sequence developed for the device to be tested (page 25, 2<sup>nd</sup> column, lines 1-2; figure 4).

As to claim 10, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the representation of the device is created within an interface module, and the step (b) of generating the test environment includes mapping signals within the interface module to signals within the test environment, the mapping being defined within the configuration file (page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

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Referring to claim 11, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the configuration file identifies a level of hierarchy of the representation of the device within the interface module to facilitate the mapping of signals (page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

As to claim 12, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, further comprising the step of: providing a trickbox component compatible with the bus protocol and provided with a general-purpose input/output interface (figures 2 and 4).

Referring to claim 13, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the type of device that may be tested comprises a master, a slave, an arbiter or a decoder (figure 1, "TXD/RXD").

As to claim 14, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the bus protocol is the ARM AMBA bus protocol, the bus comprises a system bus and a peripheral bus, and the type of device which may be tested comprises a system bus master, a system bus slave, a peripheral bus master, a peripheral bus slave, an arbiter or a decoder (figure 1, "TXD/RXD").

Referring to claim 15, Kishi et al. disclose a method of testing compliance of a device with a bus protocol, wherein the representation of the device is a Register Transfer Language (RTL) representation (page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4).

As to claim 16, Kishi et al. disclose a computer program operable to configure a processing unit to perform a method of testing compliance of a device as claimed in Claim 1 (Photo 2).

Referring to claim 17, Kishi et al. disclose a carrier medium comprising a computer program as claimed in Claim 16 (Photo 2).

As to claim 18, Kishi et al. disclose a data processing system for testing compliance of a device with a bus protocol, the system comprising: memory for storing a configuration file containing predetermined parameters identifying the type of the device and capabilities of the device (figure 4, "SDRAM, ROM/FLASH, SRAM), and a processing unit (figure 4, "Test environment of  $\mu$ PLATcore-7C based system LSI) arranged to perform the steps of: (i) dynamically generating a test environment for the device by creating selected test components which are coupled via the bus with a representation of the device to form the test environment, the test components being selected dependent on the configuration file (figure 1, "Block diagram of  $\mu$ PLATcore-7C; figure 4, "Test environment of  $\mu$ PLATcore-7C based system LSI); (ii) executing a test sequence (figure 4, "Test environment of  $\mu$ PLATcore-7C based system LSI); and (iii) monitoring signals passed between the representation of the device and one or more of the test components during execution of the test sequence to generate result data indicating compliance with the bus protocol (page 25, 1<sup>st</sup> column: Section 3.3 IP Product Line Up, lines 1-7; 2<sup>nd</sup> column, lines 1-2; page 26, 2<sup>nd</sup> column: Section 4.2 Test Bench, lines 1-8; figure 4; Photos 1-2).

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,366,973 to Lo et al.

U.S. Patent No. 6,581,019 to Bapst et al.

U.S. Patent No. 6,574,691 to Jirgal et al.

U.S. Patent No. 6,425,071 to Lo et al.



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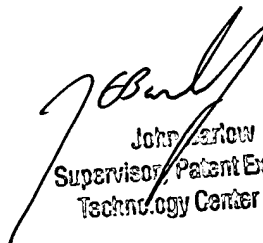
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M Le whose telephone number is (703) 305-4016. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (703) 308-3126. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.

Toan Le

December 10, 2003

  
John Barlow  
Supervisor, Patent Examiner  
Technology Center 2800